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EXAMINER	
JEFFERSON, QUOVAUNDA	

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,001	LEE ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29,31,32 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29,31,32 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 26, 2006 has been entered.

Claim Objections

Claims 1, 5, 6, 7, 8, 12, 16, 17, 21, 25, and 26 are objected to because of the following informalities. Appropriate correction is requested.

The term "attack barrier layer" in claims 1, 5, 6, 7, 8, 12, 16, 17, 21, 25, and 26 is generally narrative and indefinite, failing to conform to current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. Examiner is unsure why applicant has chosen the term “attack barrier layer” and how if differs from the term “barrier layer”, which is typically used in the art. Does this “attack barrier layer” differ from a “barrier layer” or

any other type of barrier layer that may be used? Examiner suggests changing the term "attack barrier layer" to "barrier layer".

The term "a lost portion of the etch stop layer" in claims 1, 12, and 21 is generally narrative and indefinite, failing to conform to current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. The claim does not explain how the portion of the etch stop layer is lost, which gives the inference that the portion of the etch stop layer is just misplaced. Examiner suggests adding how the portion of the etch stop layer is lost to the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-20, 31, 32, and 36 rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (herein referred to as AAPA) in view of Kawai, US Patent Application Publication 2003/0137051.

Regarding claim 1, AAPA discloses a method for fabricating a semiconductor device, comprising the steps of forming an etch stop layer **S** having a multi-layer

structure along a profile containing conductive patterns **G** formed on a substrate, etching selectively a first inter-layer insulation layer **14** deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate allocated between the conductive patterns (Figure 1A), forming a first plug **17** by depositing a conductive layer on an entire surface of the resulting structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer and the etch stop layer at the same plane level of the conductive patterns (Figure 1B), performing a cleaning process to remove remnants from the planarization process (page 5, lines 6-19), etching selectively a second inter-layer insulation layer **18** deposited along a profile containing the first plug to form a second contact hole exposing the first plug (Figure 1C); and forming a second plug electrically connected to the first plug through the second contact hole (Figure 1D).

AAPA fails to teach forming an attack barrier layer above the etch stop layer exposed by the second contact hole, wherein a lost portion of the etch stop layer is filled with a portion of the attack barrier layer.

Kawai teaches forming an attack barrier layer **24** above the etch stop layer exposed by the second contact hole, wherein a lost portion of the etch stop layer is filled with a portion of the attack barrier layer (Note: This is taught by Kawai when using the device as taught in figure 1B by AAPA and adding the barrier layer of 24 of Kawai) as a means of forming two conductive plugs that are electrically connected with each other

and because layer 24 (called an etch prevention layer) has a high etch selectivity rate with respect to the first insulating layer the second contact hole is stopped to be etched in a surface of the first etching prevention film, which means that the second contact hole would never etch further than this etching prevention layer (Kawai, [0142]).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Kawai with that of AAPA as a means of forming two conductive plugs that are electrically connected with each other and because layer 24 (called an etch prevention layer) has a high etch selectivity rate with respect to the first insulating layer the second contact hole is stopped to be etched in a surface of the first etching prevention film, which means that the second contact hole would never etch further than this etching prevention layer (Kawai, [0142]).

Regarding claim 2, AAPA further teaches the multilayer structure of the etch stop layer includes nitride layers as top and bottom most layers and at least one insulating material-based layer being disposed between the nitride layer and having a lower dielectric constant than those of the nitride layers (page 2, line 22).

Regarding claim 3, AAPA further teaches the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell

region and a CMP process prior to the step of performing the SAC etching process for forming the first contact hole (page 4, lines 1-25).

Regarding claim 4, AAPA and Kawai fail to teach the thickness of the first inter layer insulation layer and the etch stop layer disposed on each conductive pattern ranges from about 500 Angstroms to about 1500 Angstroms. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 5, Kawai further teaches after the step of performing the cleaning process, the attack barrier layer is deposited on an entire surface of the profile containing the first plug (figure 16a).

Regarding claim 7, Kawai further teaches the attack barrier layer is a nitride-based layer [0140].

Regarding claim 8, Kawai further teaches the attack barrier layer has a thickness ranging from about 50 A to about 500 A [0140].

Regarding claim 9, AAPA further teaches the insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an aluminum oxide (Al_2O_3) layer and a tantalum oxynitride (TaON) layer (page 2, line 22).

Regarding claim 10, AAPA further teaches the cleaning process uses a cleaning solution of hydrofluoric acid (HF) or buffered oxide etchant (BOE) (page 5, lines 19).

Regarding claim 11, AAPA further teaches the conductive pattern G is a gate electrode pattern and the second plug 22 is a storage node contact plug (page 2, line 26 and page 8, line 9.

Regarding claim 12, AAPA discloses a method for fabricating a semiconductor device, comprising the steps of forming an etch stop layer S having a multi-layer structure along a profile containing conductive patterns G formed on a substrate, etching selectively a first inter-layer insulation layer 14 deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate allocated between the conductive patterns (Figure 1 A), forming a first plug 17 by depositing a conductive layer on an entire surface of a structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer and the etch stop layer at the same plane level of the conductive patterns (Figure 1 B), and performing a cleaning process to remove remnants from the planarization process (page 5, lines 6-19).

AAPA fails to teach forming an attack barrier layer on an entire surface of the resulting structure including the first plug, a second inter-layer insulation layer formed on the attack barrier layer and etching selectively the attack barrier layer and forming a second plug electrically connected to the first plug through the second contact hole,

wherein a lost portion of the etch stop layer removed during the cleaning process is filled with a portion of the attack barrier layer.

Kawai teaches forming an attack barrier layer **24** on an entire surface of the resulting structure including the first plug 7 (figure 16a), a second inter-layer insulation layer 8 formed on the attack barrier layer and etching selectively the attack barrier layer (figure 16b) and forming a second plug 10 electrically connected to the first plug through the second contact hole, wherein a lost portion of the etch stop layer removed during the cleaning process is filled with a portion of the attack barrier layer (Note: This is taught by Kawai when using the device as taught in figure 1B by AAPA and adding the barrier layer of 24 of Kawai) as a means of forming two conductive plugs that are electrically connected with each other and because layer 24 (called an etch prevention layer) has a high etch selectivity rate with respect to the first insulating layer the second contact hole is stopped to be etched in a surface of the first etching prevention film, which means that the second contact hole would never etch further than this etching prevention layer (Kawai, [0142]).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Kawai with that of AAPA as a means of forming two conductive plugs that are electrically connected with each other and because layer 24 (called an etch prevention layer) has a high etch selectivity rate with respect to the first insulating layer the second contact hole is stopped to be etched in a surface of the first

etching prevention film, which means that the second contact hole would never etch further than this etching prevention layer (Kawai, [0142]).

Regarding claim 13, AAPA further teaches the multilayer structure of the etch stop layer includes nitride layers as top and bottom most layers and at least one insulating material-based layer being disposed between the nitride layer and having a lower dielectric constant than those of the nitride layers (page 2, line 22).

Regarding claim 14, AAPA further teaches the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell region and a CMP process prior to the step of performing the SAC etching process for forming the first contact hole (page 4, lines 1-25).

Regarding claim 15, AAPA and Kawai fail to teach the thickness of the first inter layer insulation layer and the etch stop layer disposed on each conductive pattern ranges from about 500 Angstroms to about 1500 Angstroms. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results

arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 16, Kawai further teaches the attack barrier layer is a nitride-based layer [0140].

Regarding claim 17, Kawai further teaches the attack barrier layer has a thickness ranging from about 50 Angstroms to about 500 Angstroms [0140].

Regarding claim 18, AAPA further teaches the insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an aluminum oxide (Al_2O_3) layer and a tantalum oxynitride (TaON) layer (page 2, line 22).

Regarding claim 19, AAPA further teaches the cleaning process uses a cleaning solution of hydrofluoric acid (HF) or buffered oxide etchant (BOE) (page 5, lines 19).

Regarding claim 20, AAPA further teaches the conductive pattern G is a gate electrode pattern and the second plug 22 is a storage node contact plug (page 2, line 26 and page 8, line 9.

Regarding claim 31, AAPA further teaches the second inter-layer insulation layer has a flow-fill property (page 4, line 22 to page 5, line 11).

Regarding claim 32, AAPA further teaches the second inter-layer insulation layer is made of an oxide-based material selected from a group consisting of advanced planarization layer (APL), spin on dielectric (SOD), spin on glass (SOG) and borophosphosilicate glass (BPSG) (page 4, line 22 to page 5, line 11).

Regarding claim 36, Kawai further teaches the second inter-layer insulation layer has a thickness ranging from about 1000 A to about 8000 A [0090].

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Kawai as applied to claim 1 above, and further in view of DeBoer et al, US Patent 6,696,336.

Regarding claim 6, AAPA and Kawai fail to teach after the step of forming the second contact hole, the attack barrier layer is formed along a profile containing the second contact hole. However, DeBoer teaches after the step of forming the second contact hole, the attack barrier layer **80, 82** is formed along a profile containing the second contact hole as protection layers, further protecting the interlayer insulating layer **24** from the conductive plug **94** to be formed (figure 8 and column 3, lines 1-15)

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of DeBoer with that of AAPA and Kawai because the attack barrier layers of DeBoer serve as protection layers, further protecting the interlayer insulating layer **24** from the conductive plug **94** to be formed.

Claims 21-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and DeBoer et al, US Patent 6,696,336 (as previously cited).

Regarding claim 21, AAPA discloses a method for fabricating a semiconductor device, comprising the steps of forming an etch stop layer **S** having a multi-layer structure along a profile containing conductive patterns **G** formed on a substrate (Figure 1A), etching selectively a first inter-layer insulation layer **14** deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate allocated between the conductive patterns (Figure 1 A), forming a first plug **17** by depositing a conductive layer on an entire surface of a structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer and the etch stop layer at the same plane level of the conductive patterns and the first inter-layer insulation layer by employing a CMP process, performing a cleaning process to remove remnants from the planarizing process (page 5, lines 6-19) and etching selectively a second inter-layer insulation layer deposited on the resulting structure including the first plug to form a second contact hole exposing the first plug (Figure 1 C),

AAPA fails to teach forming an attack barrier layer along a profile containing the second contact hole, removing the attack barrier layer disposed at a bottom surface of the second contact hole through an etch-back process and forming a second plug electrically connected to the first plug through the second contact hole, wherein a lost portion of the etch stop layer removed during the cleaning process is filled with a portion of the attack barrier layer.

DeBoer teaches forming an attack barrier layer **80, 82** along a profile containing the second contact hole (figure 8), removing the attack barrier layer disposed at a bottom surface of the second contact hole through an etch-back process (figure 9) and forming a second plug **94** electrically connected to the first plug **20** through the second contact hole, wherein a lost portion of the etch stop layer removed during the cleaning process is filled with a portion of the attack barrier layer as protection layers, further protecting the interlayer insulating layer **24** from the conductive plug **94** to be formed (figure 8 and column 3, lines 1-15 Note: Using the figure 1B as disclosed by AAPA with the lost portions of etch stop layer and substituting that into for the portion below the BPSG layer **24** of DeBoer, the profile of the bottom portion of the figure would then have the lost etch stop layers as shown in AAPA, figure 1B. Therefore, when layers 80 and 82 are added, as shown in figure 8, part of those layers would fall into the lost portions of the etch stop layer. In addition, when the layers 80 and 82 are etched from the bottom of the second contact hole and the profile of the bottom of the contact hole is smoothed out, there would still be some part of layers 80 and 82 next to the conductive plug since its profile was uneven in the beginning).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of DeBoer with that of AAPA because the attack barrier layers of DeBoer serve as protection layers, further protecting the interlayer insulating layer **24** from the conductive plug **94** to be formed.

Regarding claim 22, AAPA further teaches the multi-layer structure of the etch stop layer includes nitride layers as top and bottom most layers and at least one insulating material-based layer being disposed between the nitride layers and having a lower dielectric constant than those of the nitride layers (page 2, line 22).

Regarding claim 23, AAPA further teaches the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell region and a CMP process prior to the step of performing the SAC etching process for forming the first contact hole (page 4, lines 1-25).

Regarding claim 24, AAPA and DeBoer fail to teach the thickness of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern preferably ranges from about 500 Angstoms to about 1500 Angstroms. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See In re Aller, Lacey, and Hall (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile

chosen dimensions are critical. In re Woodruff; 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. Ex parte Ishizaka, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. In re Burckel, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 25, DeBoer further teaches the attack barrier layer is a nitride-based layer (column 4, line 59).

Regarding claim 26, DeBoer further teaches the attack barrier layer has a thickness ranging from about 50 A to about 500 A (column 4, line 60).

Regarding claim 27, AAPA further teaches the insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an Al203 layer and a TaON layer (page 2, line 22).

Regarding claim 28, AAPA further teaches the method as recited in claim 21, wherein the cleaning process uses a cleaning solution of HF or BOE (page 5, line 9).

Regarding claim 29, AAPA further teaches the method as recited in claim 21, wherein the conductive pattern S is a gate electrode pattern and the second plug 22 is a storage node contact plug (page 2, line 26 and page 8, line 9).

Response to Arguments

Applicant's arguments with respect to claims 1-20, 31, 32, and 36 have been considered but are moot in view of the new ground(s) of rejection.

Regarding independent claim 21, Applicant argues that the amended limitation of "forming a second plug electrically connected to the first plug through the second contact hole, wherein a lost portion of the etch stop layer removed during the cleaning process is filled with a portion of the attack barrier layer" is not taught by the cited

references of Applicant's Admitted Prior Art (AAPA) or DeBoer et al. Applicant contends that DeBoer does not teach or suggest that layers 80 and 82 fill in a lost portion of any underlying layers. In addition, applicant states that "although misalignment occurs when a contact hole is formed, the layers 80 and 82 cannot fill into a partial region of the sidewall space layer of the gate pattern removed by misalignment of the contact due to the oxide layer **22**." on page 11 of Applicant's Remarks.

In response to these arguments, Examiner points out that the newly amended limitation "forming a second plug electrically connected to the first plug through the second contact hole, wherein a lost portion of the etch stop layer removed during the cleaning process is filled with a portion of the attack barrier layer" is taught by DeBoer by substitution of AAPA. Using the figure 1B as disclosed by AAPA with the lost portions of etch stop layer and substituting that into for the portion below the BPSG layer **24** of DeBoer, the profile of the bottom portion of the figure would then have the lost etch stop layers as shown in AAPA, figure 1B. Therefore, when layers 80 and 82 are added, as shown in figure 8, part of those layers would fall into the lost portions of the etch stop layer. In addition, when the layers 80 and 82 are etched from the bottom of the second contact hole and the profile of the bottom of the contact hole is smoothed out, there would still be some part of layers 80 and 82 next to the conductive plug since its profile was uneven in the beginning. Therefore, the rejection of claim 21 of AAPA in view of DeBoer is deemed proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fernando Toledo
Patent Examiner
Art Unit 2823

QVJ